UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,377	12/29/2000	Anthony X. Jarvis	00-BN-055 (STMI01-00055)	8283

30425 7590 04/27/2004

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,377	JARVIS, ANTHONY X.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 3/15/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi, U.S. Patent No. 5,805,852.

7. Regarding claim 1, Nakanishi has taught a data processor comprising:

a. An instruction execution pipeline comprising:

i. A read stage ("MEM" stage, see Col.9 lines 13-23),

ii. A write stage ("WB" stage, see Col.9 lines 13-23),

iii. A first execution stage ("EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (see "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

b. A register file (5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (see Col.9 lines 53-56) via at least one of R read ports of said register file (see Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (see Col.9 lines 61-64) via at least one of W write ports of said register file (see Col.9 lines 5-9),

c. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising a first plurality of bypass tri-state line drivers having input channels coupled to first output channels of a first plurality of said source devices and tri-state output channels coupled to a first common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

d. A first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first

execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

8. Regarding claim 2, Nakanishi has taught the data processor as set forth in claim 1 above, wherein said bypass circuitry further comprises a second plurality of bypass tri-state line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tri-state output channels coupled to a second common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

9. Regarding claim 3, Nakanishi has taught the data processor as set forth in claim 2 above, further comprising a first register file tri-state line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

10. Regarding claim 4, Nakanishi has taught the data processor as set forth in claim 3 above, further comprising a second register file tri-state line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

11. Regarding claim 6, Nakanishi has taught the data processor as set forth in claim 4 above, further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-

state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

12. Regarding claim 7, Nakanishi has taught the data processor as set forth in claim 6 above, wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as a multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

13. Regarding claim 8, Nakanishi has taught the data processor as set forth in claim 7 above, wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

14. Regarding claim 9, Nakanishi has taught the data processor as set forth in claim 8 above, wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

15. Regarding claim 10, Nakanishi has taught the data processor as set forth in claim 9 above, wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

16. Regarding claim 21, Nakanishi has taught the processing system of claim 1, further comprising a latch (see L1-L8 of Fig.3) coupled to the output channel of the first multiplexer and to the first operand channel of the first execution unit (see Col.10 lines 11-60).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 11-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent No. 5,805,852, in further view of Ferris, III et al., U.S. Patent No. 4,591,973 (hereinafter Ferris).

19. Regarding claims 11, Nakanishi has taught a processing system comprising:

a. A data processor (see Fig.1), wherein said data processor comprises:

I. An instruction execution pipeline comprising:

i. A read stage ("MEM" stage, see Col.9 lines 13-23),

ii. A write stage ("WB" stage, see Col.9 lines 13-23),

iii. A first execution stage ("EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (see "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

II. A register file (5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (see Col.9 lines 53-56) via at least one of R read ports of said register file (see Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (see Col.9 lines 61-64) via at least one of W write ports of said register file (see Col.9 lines 5-9),

III. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:

i. A first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

ii. A first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

b. A memory coupled to said data processor (1 of Fig.1).

20. Nakanishi has not explicitly taught a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

21. However, Ferris has taught a plurality of memory-mapped peripheral circuits coupled to a data processor (see Fig.1, Col.1 lines 43-52, and Col.3 lines 3-19) in order to decrease the burden on the main processor and provide greater throughput and performance (see Col.1 lines 21-31). One of ordinary skill in the art would have recognized that increasing the performance of microprocessor systems is a primary goal of their designers. Therefore, one of ordinary skill in the art would have found it obvious to modify Nakanishi to include a plurality of memory-mapped peripheral circuits in order to increase the performance of the processor (see Col.1 lines 21-31).

22. Regarding claim 12, Nakanishi in view of Ferris has taught the processing system as set forth in claim 11 above, wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said

first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage (see Nakanishi, Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

23. Regarding claim 13, Nakanishi in view of Ferris has taught the processing system as set forth in claim 12 above, further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (see Nakanishi, Fig.3, and Col.10 lines 48-60).

24. Regarding claim 14, Nakanishi in view of Ferris has taught the processing system as set forth in claim 13 above, further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (see Nakanishi, Fig.3, and Col.10 lines 48-60).

25. Regarding claim 16, Nakanishi in view of Ferris has taught the processing system as set forth in claim 14 above, further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (see Nakanishi, Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

26. Regarding claim 17, Nakanishi in view of Ferris has taught the processing system as set forth in claim 16 above, wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer

(see Nakanishi, Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as a multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

27. Regarding claim 18, Nakanishi in view of Ferris has taught the processing system as set forth in claim 17 above, wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (see Nakanishi, Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

28. Regarding claim 19, Nakanishi in view of Ferris has taught the processing system as set forth in claim 18 above, wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (see Nakanishi, Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

29. Regarding claim 20, Nakanishi in view of Ferris has taught the processing system as set forth in claim 19 above, wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (see Nakanishi, Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage

that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

30. Regarding claim 22, Nakanishi in view of Ferris has taught the processing system of claim 11, further comprising a latch (see Nakanishi, L1-L8 of Fig.3) coupled to the output channel of the first multiplexer and to the first operand channel of the first execution unit (see Nakanishi, Col.10 lines 11-60).

Response to Arguments

31. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. However, the Examiner would like to address the following arguments presented by the Applicant.

32. On pages 11 and 12 of the instant application, the Applicant argues, in essence:

"Nakanishi simply recites a mechanism for using tri-state buffers to supply a particular data value to a specific bus, thereby providing the data value to a specific latch circuit in the processor of Nakanishi. Nakanishi lacks any mention of using multiplexers with the tri-state buffers...In fact, the tristate buffers of Nakanishi ensure that only one data value is supplied to any single bus in the processor at any particular time, so there is no actual need for multiplexers in the processor Nakanishi. Because of this, this portion of

Nakanishi fails to recite 'bypass circuitry' that includes both a 'plurality of bypass tristate line drivers' and a 'multiplexer' as recited in claim 1."

33. The Examiner would like to point out that the function of the tri-state buffer network of the Nakanishi reference that the Applicant states, specifically that they "*ensure that only one data value is supplied to any single bus in the processor at any particular time*", is the definition of the function of a multiplexer. For example, the textbook Computer Organization & Design: The Hardware/Software Interface by Patterson and Hennessy defines the function of a multiplexer as selecting one of its plurality of inputs to be applied to its output (see p.B-9). Because the claim in question (claim 1) does not state any physical relationship between the "plurality of bypass tristate line drivers" and the "first multiplexer", Nakanishi has taught both a plurality of bypass tristate line drivers as well as the first multiplexer, as the first multiplexer in Nakanishi consists of a bypass network constructed of tristate drivers (see above paragraph 7).

34. Furthermore, the Examiner would like to point out that generally multiplexers are constructed using a network of tristate drivers. For example, see Acampora, U.S. Patent No. 4,982,283, which shows that preferably multiplexers are constructed using networks of tristate buffers (see Col.6 lines 56-66). This further supports the teaching of Nakanishi in showing that not only does the bypass network of tristate line drivers perform the same function as a multiplexer, it is also constructed in the manner multiplexers are generally constructed.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
4/23/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100